

Nasa CR 65376



A Report

FINAL REPORT
FOR
PREMODULATION FILTERS

SCI PART NO. 1185001-1

CONTRACT NAS9-4393

TO

NASA
MANNED SPACEFLIGHT CENTER

HOUSTON, TEXAS

APRIL 1966

FACILITY FORM 608

N66 28377

(ACCESSION NUMBER)

(THRU)

17

(PAGES)

1

(CODE)

CR-65376

(NASA CR OR TMX OR AD NUMBER)

09

(CATEGORY)

GPO PRICE \$ _____

CFSTI PRICE(S) \$ _____

Space Craft, Inc.

Hard copy (HC) 1.00

Microfiche (MF) .50

TABLE OF CONTENTS

1.0	INTRODUCTION
2.0	CIRCUIT DESCRIPTION
2.1	Voltage Regulator
2.2	DC to DC Inverter
2.3	Input Buffer
2.4	Toggled Flip-Flop
2.5	Filter Circuits
2.6	Output Buffers
3.0	CIRCUIT OPERATION SUMMARY
4.0	EXPLANATION OF DOCUMENTATION
5.0	TEST RESULTS

1.0 INTRODUCTION

The Pre-modulation Filters as designed by Space Craft Inc. consist of seven basic circuits as shown in the block diagram of figure 1. These filters employ a signal reconstruction technique. The use of this technique was dictated by the requirement for an isolated input to the filter and at the same time having the possibility of a nearly pure D.C. input signal. The method employed allows the filters to handle a D.C. signal with transformer coupling, and also provides very good noise rejection.

This report is devoted to giving the basic operation principles of each sub-circuit and its function in the overall circuit. Figure 2 is a detailed schematic diagram of the 800 Bit/sec pre-modulation filter.

2.0 CIRCUIT DESCRIPTION

2.1 Voltage Regulator

The specified output amplitude tolerances and operating voltage specifications require that internal regulation and filtering of the circuit operating voltages be provided. This is accomplished by the power regulator shown in figures 1 and 2. The regulator used is a Darlington connected series type regulator. CR2 is the internal voltage reference and Q2 acting as a comparator, and compares the feedback voltage to the reference to produce a control signal for the regulating devices, Q1 and Q23. Input filtering is used to minimize current feedback into the 28 vdc source and to aid the regulator in smoothing the input voltage. Diode CR1 furnishes reverse polarity protection and which with C1 produces a peak reading action that improves the rejection of ripple on the 28 vdc line.

2.2 DC to DC Inverter

To satisfy the requirement for a d.c. isolated input, isolated operating voltages are required for the input buffer circuit. These voltages are provided by a DC-DC converter consisting of a free-running multivibrator, transformer T1, and diodes CR13 and CR14. The multivibrator is basically standard in its design. Q3 and Q5 and diodes CR3 and CR4 form a standard emitter follower pull-up circuit to decrease the rise time of the circuit to acceptable limits. Diodes

CR8 and CR9 protect the base-emitter junctions, and together with resistors R52 and R53 aid in the self-starting ability of the multi-vibrator. A charge transfer circuit is incorporated to generate a negative voltage required by other circuitry. Both the charge transfer circuit and transformer T1 are driven by a push-pull method. This use of full wave rectifying techniques greatly reduces the filtering requirements of the inverter output voltages as well as reducing feedback to the regulated B+ lines. Resistor R6 and capacitor C5 provide isolation and filtering of the B+ line to the inverter circuit.

2.3 Input Buffer

The input buffer stage is a conventional high input impedance, unity gain, low output impedance amplifier. Resistor R14 is included to reduce voltage noise that appears when used with high impedance signal sources. With high source impedances noise is present due to stray capacitive coupling of high-frequency signal components back to the input line. Resistor R14 and stray capacitance at the base of Q7 also act as a filter against unwanted high-frequency input noise. Capacitor C14 is used to prevent high-frequency instability of the input buffer. Coupling capacitor C15 and transformer T2 form a differentiating circuit that provides fast voltage spikes used to trigger the toggled flip-flop, at the same time isolating the input-signal common from other commons in the system.

2.4 Toggled Flip-Flop

The toggled flip-flop is a fairly conventional complementary flip-flop. When power is applied to the pre-modulation filter, and no input signal is present, the flip-flop output will go to its most negative state. Resistor R55 in parallel with the load resistance is the determining component in the initial state of the flip-flop. With R55 being smaller than R23, Q11 will receive a stronger initial forward biasing current than is possible for Q13, therefore Q11 will turn on bringing Q14 on with it. The regenerative action of the circuit then results in Q12 and Q14 turning off. The flip-flop will remain in this state until a positive voltage pulse is received from the lower section of the transformer T2 secondary winding through CR19. This pulse tends to turn off Q11 lowering its collector voltage and causing Q13 to turn on. Regenerative action then quickly continues the transition bringing the output of the flip-flop positive. Transition time of the flip-flop is less than 100 nanoseconds in both directions. Because of the fast transition time of the flip-flop only very small current spikes are generated on the B+ line. Capacitor C17 is provided to absorb whatever current spikes are generated. Resistors R16 and R17 provide DC biasing on the secondary of transformer T2 to determine the minimum amplitude of the triggering pulses needed to trigger the toggled flip-flop. Very good signal to noise rejection is possible with this method since no signal below the preset level can trigger the flip-flop. Very good signal to noise rejection is possible with this method since no signal below the preset level can trigger the flip-flop. A signal to noise rejection ratio approaching unity is possible, however a ratio considerably less than unity was chosen in order to

ensure reliable operation. Diode CR18 provides temperature stability of the biasing point, and capacitor C16 filters out any AC components. Immunity to low frequency noise is provided by the differentiating action of C15 - T2.

2.5 Filter Circuits

The output of the flip-flop is fed into a 6th order active filter. The amplifiers used in each section are of standard design. Each is a unity gain, high input impedance, low output impedance circuit. Each section is of a 3rd order configuration. Components values for the filter were first calculated and then adjusted empirically on the headboard model to obtain optimum results with standard values. Once component values were determined for one frequency, direct frequency scaling was used to obtain other values for filters of other bit rates. The frequency response characteristics of the filter circuits is calculated to be of the Buttersworth-Thompson form, giving a compromise of the flatness of the Buttersworth and the linear time delay of the Bessel types. Close tolerance capacitors and resistors are necessary in the filter sections to eliminate the need for selecting components for the different bit-rate filters.

The output of the filters section is direct coupled to two output buffers which furnish the two specified output signals.

2.6 Output Buffers

The output No. 2 buffer is a standard "cascode doublet" unity gain amplifier. The output amplitude is determined by adjusting resistor

R45, and is one of the component selections necessary during the manufacturing process. Diode CR24 provides temperature compensation for V_{BE} drift. Short circuiting output No. 2 to ground will not cause the current drawn by this stage to increase above its normal operating maximum. Long term short circuits will not damage the circuit or alter its operation when the short is removed.

The output No. 1 buffer is a similar "cascode doublet" amplifier. Resistor R49, R50 and R51 allow the gain of this buffer to be adjusted. When the buffer input is at ground potential the output voltage is negative and is a function of amplifier gain and the supply voltage at the emitter of Q21. Therefore adjusting R49 will determine the negative output voltage whenever the input voltage goes to zero. Adjusting R48 determines the maximum positive voltage of the output signal. Resistors R48 and R49 are selected during the manufacturing process. Short circuit protection is similar to that of output No. 2 buffer with resistor R35 keeping the current through Q22 at a safe level whenever the input is below the emitter voltage of Q21.

3.0 CIRCUIT OPERATION SUMMARY

Special attention was given to eliminating ground-loop problems by providing separate ground leads from the various circuits to the ground pin of the connector.

Some noise is fed into the output buffers via the supply voltages, and are present at the output. This noise apparently originates in both the inverter circuit and the toggled flip-flop circuit. Experiments with the breadboard indicate that lowering of the high frequency response of the output buffers would decrease this noise.

4.0 EXPLANATION OF DOCUMENTATION

Documentation for the pre-modulation filters is arranged for the most efficient production of the filters. Each bit-rate filter has its own part number and top assembly drawing plus the sub-assembly drawings necessary to assemble an individual bit-rate filter. This method of documentation results in a greater number of drawings than possible alternate methods but does minimize parts selection during manufacturing.

Following is a list of the top assembly drawings for each bit-rate filter and the schematics.

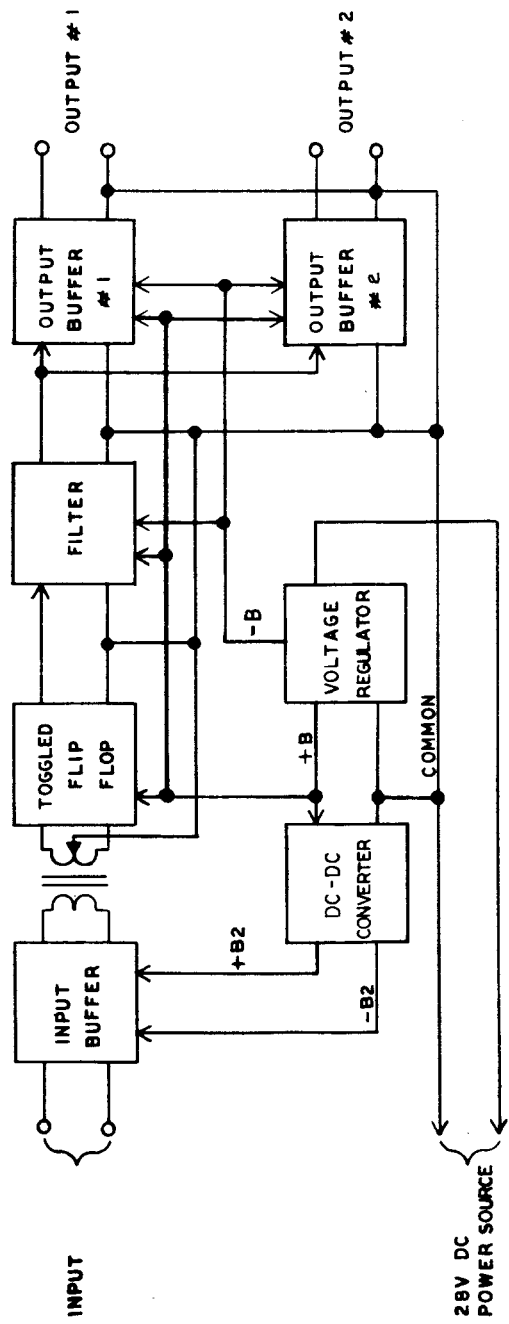
Title	Dwg. No.
Pre Modulation Filter Assembly 800 Bit/sec	1185001
Pre-Modulation Filter Assembly 1600 Bit/sec	1185019
Pre-Modulation Filter Assembly 3200 Bit/sec	1185023
Pre-Modulation Filter Assembly 6400 Bit/sec	1185027
Pre-Modulation Filter Assembly 12,800 Bit/sec	1185031
Pre-Modulation Filter Assembly 25,600 Bit/sec	1185035
Schematic Pre-Modulation Filter 800 Bit/sec	1185002
Schematic Pre-Modulation Filter 1600 Bit/sec	1185020
Schematic Pre-Modulation Filter 3200 Bit/sec	1185024

Title	Dwg. No.
Schematic Pre-Modulation Filter 6400 Bit/sec	1185028
Schematic Pre-Modulation Filter 12,800 Bit/sec	1185032
Schematic Pre-Modulation Filter 25,600 Bit/sec	1185036

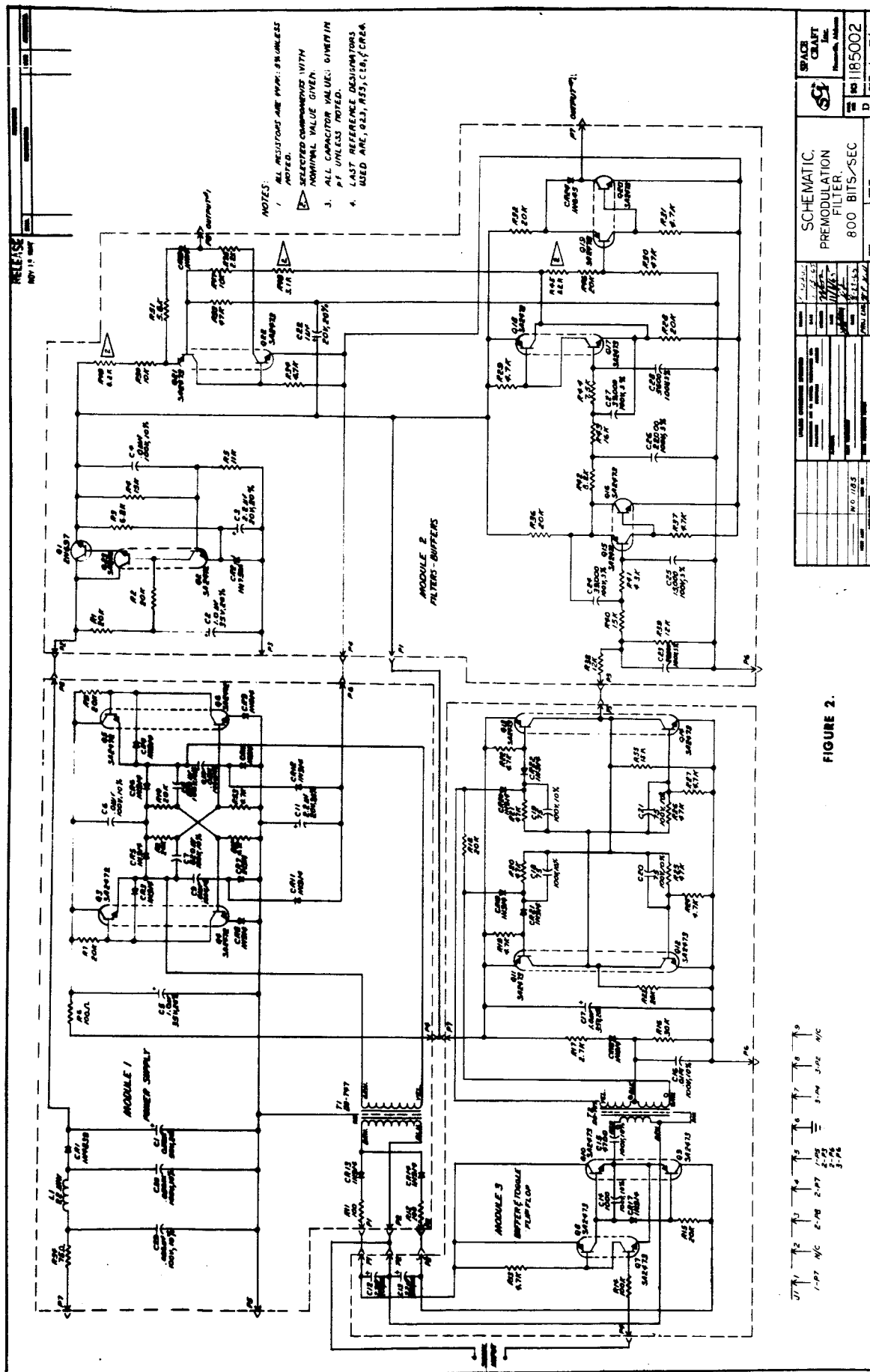
5.0 TEST RESULTS

Complete test results are given for all units in the Qualification Test Report and the Pre-Modulation Test Data Sheets.

REVISIONS			APPROVAL	
SYN.	DESCRIPTION	DATE	DATE	APPROVAL



NO. REQ'D	ITEM NO.	DESCRIPTION	MIL. SPEC.	MFR'S. PT. NO.	REMARKS/	MFR'S. CODE
LIST OF MATERIALS						
BLOCK DIAGRAM, PRE-MODULATION FILTER FIGURE 1						
SCALE NONE UNIT WT.			SCI-1185060 SHEET 1 OF 1			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES; TOLERANCES ON: FRACTIONS DECIMALS ANGLES			DRAWN JKL DATE 21 APR 66			
MATERIAL			CHECKED DATE			
HEAT TREATMENT			APPROVED DATE			
FINAL PROTECTIVE FINISH			PROJ. ENG. DATE			
APPLICATION W O I I B 5 USED ON			NEXT ASST.			



1. NAME OF THE COMPANY 2. ADDRESS 3. CITY 4. STATE 5. ZIP		6. PHONE 7. FAX 8. TELETYPE		9. NAME OF THE PERSON 10. ADDRESS 11. CITY 12. STATE 13. ZIP		14. PHONE 15. FAX 16. TELETYPE		17. NAME OF THE PERSON 18. ADDRESS 19. CITY 20. STATE 21. ZIP		22. PHONE 23. FAX 24. TELETYPE		25. NAME OF THE PERSON 26. ADDRESS 27. CITY 28. STATE 29. ZIP		30. PHONE 31. FAX 32. TELETYPE		33. NAME OF THE PERSON 34. ADDRESS 35. CITY 36. STATE 37. ZIP		38. PHONE 39. FAX 40. TELETYPE		41. NAME OF THE PERSON 42. ADDRESS 43. CITY 44. STATE 45. ZIP		46. PHONE 47. FAX 48. TELETYPE		49. NAME OF THE PERSON 50. ADDRESS 51. CITY 52. STATE 53. ZIP		54. PHONE 55. FAX 56. TELETYPE		57. NAME OF THE PERSON 58. ADDRESS 59. CITY 60. STATE 61. ZIP		62. PHONE 63. FAX 64. TELETYPE		65. NAME OF THE PERSON 66. ADDRESS 67. CITY 68. STATE 69. ZIP		70. PHONE 71. FAX 72. TELETYPE		73. NAME OF THE PERSON 74. ADDRESS 75. CITY 76. STATE 77. ZIP		78. PHONE 79. FAX 80. TELETYPE		81. NAME OF THE PERSON 82. ADDRESS 83. CITY 84. STATE 85. ZIP		86. PHONE 87. FAX 88. TELETYPE		89. NAME OF THE PERSON 90. ADDRESS 91. CITY 92. STATE 93. ZIP		94. PHONE 95. FAX 96. TELETYPE		97. NAME OF THE PERSON 98. ADDRESS 99. CITY 100. STATE 101. ZIP		102. PHONE 103. FAX 104. TELETYPE		105. NAME OF THE PERSON 106. ADDRESS 107. CITY 108. STATE 109. ZIP		110. PHONE 111. FAX 112. TELETYPE		113. NAME OF THE PERSON 114. ADDRESS 115. CITY 116. STATE 117. ZIP		118. PHONE 119. FAX 120. TELETYPE		121. NAME OF THE PERSON 122. ADDRESS 123. CITY 124. STATE 125. ZIP		126. PHONE 127. FAX 128. TELETYPE		129. NAME OF THE PERSON 130. ADDRESS 131. CITY 132. STATE 133. ZIP		134. PHONE 135. FAX 136. TELETYPE		137. NAME OF THE PERSON 138. ADDRESS 139. CITY 140. STATE 141. ZIP		142. PHONE 143. FAX 144. TELETYPE		145. NAME OF THE PERSON 146. ADDRESS 147. CITY 148. STATE 149. ZIP		150. PHONE 151. FAX 152. TELETYPE		153. NAME OF THE PERSON 154. ADDRESS 155. CITY 156. STATE 157. ZIP		158. PHONE 159. FAX 160. TELETYPE		161. NAME OF THE PERSON 162. ADDRESS 163. CITY 164. STATE 165. ZIP		166. PHONE 167. FAX 168. TELETYPE		169. NAME OF THE PERSON 170. ADDRESS 171. CITY 172. STATE 173. ZIP		174. PHONE 175. FAX 176. TELETYPE		177. NAME OF THE PERSON 178. ADDRESS 179. CITY 180. STATE 181. ZIP		182. PHONE 183. FAX 184. TELETYPE		185. NAME OF THE PERSON 186. ADDRESS 187. CITY 188. STATE 189. ZIP		190. PHONE 191. FAX 192. TELETYPE		193. NAME OF THE PERSON 194. ADDRESS 195. CITY 196. STATE 197. ZIP		198. PHONE 199. FAX 200. TELETYPE		201. NAME OF THE PERSON 202. ADDRESS 203. CITY 204. STATE 205. ZIP		206. PHONE 207. FAX 208. TELETYPE		209. NAME OF THE PERSON 210. ADDRESS 211. CITY 212. STATE 213. ZIP		214. PHONE 215. FAX 216. TELETYPE		217. NAME OF THE PERSON 218. ADDRESS 219. CITY 220. STATE 221. ZIP		222. PHONE 223. FAX 224. TELETYPE		225. NAME OF THE PERSON 226. ADDRESS 227. CITY 228. STATE 229. ZIP		230. PHONE 231. FAX 232. TELETYPE		233. NAME OF THE PERSON 234. ADDRESS 235. CITY 236. STATE 237. ZIP		238. PHONE 239. FAX 240. TELETYPE		241. NAME OF THE PERSON 242. ADDRESS 243. CITY 244. STATE 245. ZIP		246. PHONE 247. FAX 248. TELETYPE		249. NAME OF THE PERSON 250. ADDRESS 251. CITY 252. STATE 253. ZIP		254. PHONE 255. FAX 256. TELETYPE		257. NAME OF THE PERSON 258. ADDRESS 259. CITY 260. STATE 261. ZIP		262. PHONE 263. FAX 264. TELETYPE		265. NAME OF THE PERSON 266. ADDRESS 267. CITY 268. STATE 269. ZIP		270. PHONE 271. FAX 272. TELETYPE		273. NAME OF THE PERSON 274. ADDRESS 275. CITY 276. STATE 277. ZIP		278. PHONE 279. FAX 280. TELETYPE		281. NAME OF THE PERSON 282. ADDRESS 283. CITY 284. STATE 285. ZIP		286. PHONE 287. FAX 288. TELETYPE		289. NAME OF THE PERSON 290. ADDRESS 291. CITY 292. STATE 293. ZIP		294. PHONE 295. FAX 296. TELETYPE		297. NAME OF THE PERSON 298. ADDRESS 299. CITY 300. STATE 301. ZIP		302. PHONE 303. FAX 304. TELETYPE		305. NAME OF THE PERSON 306. ADDRESS 307. CITY 308. STATE 309. ZIP		310. PHONE 311. FAX 312. TELETYPE		313. NAME OF THE PERSON 314. ADDRESS 315. CITY 316. STATE 317. ZIP		318. PHONE 319. FAX 320. TELETYPE		321. NAME OF THE PERSON 322. ADDRESS 323. CITY 324. STATE 325. ZIP		326. PHONE 327. FAX 328. TELETYPE		329. NAME	
---	--	-----------------------------------	--	--	--	--------------------------------------	--	---	--	--------------------------------------	--	---	--	--------------------------------------	--	---	--	--------------------------------------	--	---	--	--------------------------------------	--	---	--	--------------------------------------	--	---	--	--------------------------------------	--	---	--	--------------------------------------	--	---	--	--------------------------------------	--	---	--	--------------------------------------	--	---	--	--------------------------------------	--	---	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	--	--	---	--	-----------	--